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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,738	WOLRICH ET AL.	
	Examiner	Art Unit	
	NGOC V. DINH	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,13,14,16-21,26-29,31-35,37-41 and 43-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13,16-21,26-29,31,40 and 43-48* is/are rejected.

7)☐ Claim(s) *14,32-35,37-39 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

DETAILED ACTION

1. This Office Action is responsive to Amendment filed 07/15/05. Claims 8-12, 15, 22-25, 30, 36, 42 are canceled.

Applicant's arguments filed 07/15/05 have been considered by the Examiner and are deemed persuasive. Accordingly, the rejection of claims 1-7, 13-14,16-21, 26-48 based on Adiletta and Patka et al in the office letter dated 07/15/05 is respectfully withdrawn and the following rejection based on Singhal et al is applicable.

INFORMATION DISCLOSURE STATEMENT

2. The Applicant's submission of the IDS filed 07/15/05 have been considered. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 is attached to the instant office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-7, 13, 16-19, 21, 26-28, 31, 43-48 are rejected under 35 U.S.C 103(a) as being unpatentable over Singhal et al PN 5,978,874.

Per claim 1:

Singhal teaches:a method comprising:

identifying a plurality of memory resources for pushing data to and pulling data from a processing agent [e.g.; The initiator first tries to **"push" the data** to the responder by arbitrating for the Data bus and driving the data. If the responder is not ready to accept the data, it asserts DataCancel and then **"pulls" the data** by arbitrating the Data Bus and driving the appropriate DataID, col. 17, lines 20-30; col. 16, lines 15-25; col. 16, lines 62-67; col. 24, lines 49-55; col. 37, claim 13];

using a push bus arbiter [The home for the requested memory address becomes the responder. The initiator will first try to "push" the data to the responder by arbitrating for the Data bus and driving the data, col. 16, lines 62-65] to arbitrate use of **a bus** by the memory resources; pushing the data [the responder will then "pull" the data by arbitrating the Data Bus and driving the appropriate DataID. This implies that the responder tracks write-type operations that it will "pull". from the memory resources to the processing agent through the push bus, col. 16, lines 65-67] the memory resources obtaining access to **the bus** based on arbitration by the push bus arbiter;
using a pull bus arbiter [If the responder is not ready to accept the data, it asserts DataCancel and then **"pulls" the data** by arbitrating the Data Bus and driving the appropriate DataID, col. 17, lines 20-30] to arbitrate use of **a bus** by the memory resources; and pulling the data from the processing agent and transferring to the memory resources through **the bus**. the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter.

In general, Singhal teach a system and a method for arbitrating data between the processing agent [e.g., Initiator] and the memory resource [e.g., Responder] using a single bus. The initiator tries to push the data to the Responder by arbitrating for the data bus and driving the bus as a push bus [col. 16, lines 13-25]. If the responder is ready to accept the data then the Responder tries to pull the data by arbitrating the data bus and driving the bus as Pull Bus [col. 16, lines 20-30; col. 17, lines 20-30]. The Initiator/Responder try to arbitrate the bus through the arbitration unit 186 [fig. 2, col. 6, lines 1-5].

Singhal does not teach a system and a method for arbitrating data between the processing agent [e.g., Initiator] and the memory resource [e.g., Responder] using two different buses: a Push bus and a Pull bus.

It would have been obvious for one having ordinary skill in the art at the time the invention was made to use two different buses for arbitrating data between the processing agent [e.g., Initiator]

and the memory resource instead of a single bus in order to reduce number of turn-around cycles per bus, because the request and associated data are generally not sent on the same bus. Furthermore, the bandwidth in a two-bus connection is increased significantly over the single bus. The advantages of multiple buses considerably increase memory bandwidth and increase data throughput via multiple data passages.

Per claims 3, 18, 28:

the programming agent executes a context and issues a read command to a memory controller in a read phase [read-type transaction, col. 12, lines 47-65]..

Per claims 4, 19:

the memory controller processes the read command to be sent to one of the memory resources [read-type transaction, col. 12, lines 47-60].

Per claims 6-7, 21:

Singhal, inherently teaches after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer register of the programming agent, wherein after the data has been pushed, the programming agent reads the data in the input transfer register and the programming agent continues the execution of the context. This is because in the context switching process, the controller [the initiator]can process million instructions/transactions [read/write transaction] per second (MIPS) at a speed faster than a memory can provide data to the transactions. The output of the transactions after being processed must be stored in a transfer register such as buffer, read/write queue(s) and queued (delay read/write transaction) in the transfer register until the program agent [the responder] is ready to pull the output from the transfer register.

Per claim 13:

Singhal teaches a system comprising:

a plurality of memory resources [e.g., Data Out Buffer ("DOB") 186 and Data In Buffer ("DIB"), col. 29, lines 59-62; bcopy buffers or streaming IO buffers, col. 16, lines 50-55] each memory resource being associated with a memory controller [189, fig. 3];

a processing agent [180, fig. 2; Address Controller 180 generates control signals that are carried over path 190 to the Data Controller 140. Signal timings on the DataBus 70, the AddressBus/State Bus 60, the Arbitration Bus 80, and the Data ID Bus 90 are designed to permit

such multiplex-partitioning of data and address paths, col. 6, lines 23-29]to access the memory resources;

a single bus to push data from the memory resources to the processing agent ;

a push bus arbiter [col. 16, lines 62-65] to arbitrate use of **the bus** by the memory resources, the memory resources obtaining access to **the bus** based on arbitration by the push bus arbitrator;

a single bus to receive data from the processing agent and to transfer the data to the memory resources; and

a pull bus arbiter to arbitrate use of-**the bus** by the memory resources. the memorv resources obtaining access to **the bus** based on arbitration by the pull bus arbiter.

Singhal does not teach a system and a method for arbitrating data between the processing agent [e.g., Initiator] and the memory resource [e.g., Responder] using two different buses: a Push bus and a Pull bus.

The motivation for using two different buses for arbitrating scheme is already provided in claim 1.

Per claims 2, 16- 17, 27:

Singhal teaches the claimed limitations as mentioned above, and further teaches establishing a plurality of contexts on the programming agent [read/write-type transactions].

Singhal does not teach a plurality of program counters and a plurality of context relative registers, in which the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory DRAM input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers.

However, it would have been obvious for one having ordinary skill in the art at the time the invention was made to employ all circuitries as mentioned above into Singhal's computer system. These circuitries are well known in the art as hardware components which are used in instructions/transactions execution and storage.

Per claim 26:

Singhal teaches the claimed limitations as mentioned in claim 1, and further teaches a machine-accessible medium, which when accessed results in a machine performing operations [fig. 2; col. 5, line 62 to col. 6, line 20].

Per claim 31:

the programming agent executes a context and loads the data into an output transfer register of the programming agent in a write phase [write-back, col. 16, lines 3-12].

Per claims 43-48:

the memory resources comprise memory controller channels [fig. 3, 179, 185, 220,186, 187; col. 6, lines 51-65]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 20, 29, 40 are rejected under 35 U.S.C 103(a) as being unpatentable over Singhal, and in view of Dennin et al PN 6401149.

As per claims 5, 20, 29, 33, 40:

Adilleta teaches the claimed limitations as noted above.

Adilleta does not teach the context is swapped out if the read data or if the write command is required to continue the execution of the context.

Dennin teaches a context switching process in which context or task is swapped out or in if a current read or write operation is idling for its arrival data [col. 9, lines 44-50; col. 10, lines 43-60].

It would have been obvious for one having ordinary skill in the art at the time the invention was made to swap out the lower priority context in order to execute the higher priority context because the lower priority context is idle and inactive while waiting for requested data arrival. One would be motivated to process the active context while the

other context is idle and inactive for the purpose of increasing system performance [col. 2, lines 45-60].

Allowable Subject Matter

5. Claims 14, 32-35, 37-39, 41 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

NGOC DINH
Patent Examiner
ART UNIT 2189
September 28, 2005

DONALD SPARKS
SUPERVISORY PATENT EXAMINER